Data-Converter Fundamentals

Data Converter Fundamentals

- Fundamental aspects are discussed only
  - Without regard for the internal architecture or circuit design
  - Converters are treated as black boxes
  - Input-output relationships
  - Two main types of data converters, Nyquist-rate and oversampling rate
- Nyquist-rate converters
  - Nyquist-rate analog-to-digital converters (ADCs)

    Nyquist-rate digital-to analog converters (DACs)
  - Seldom used at Nyquist rate due to the difficulty in realizing practical anti-aliasing and reconstruction filters.

    In most cases, Nyquist-rate converters operate at 1.5 to 5 times the Nyquist rate (i.e, 3 to 10 times the input signal’s bandwidth).

Data Converter Fundamentals (Cont.)

- Oversampling converter
  - Oversampling ADCs and oversampling DACs
  - Operate much faster than the input signal's Nyquist rate (typical 8 to 512 times faster)
  - Noise shaping is used to place much of the quantization noise outside the input signal's bandwidth
  - Increase the output's signal-to-noise ratio (SNR) by filtering out quantization noise that is not in the signal bandwidth.

    In A/D converters, this filtering is performed digitally, whereas in D/A converters, analog filtering is used.

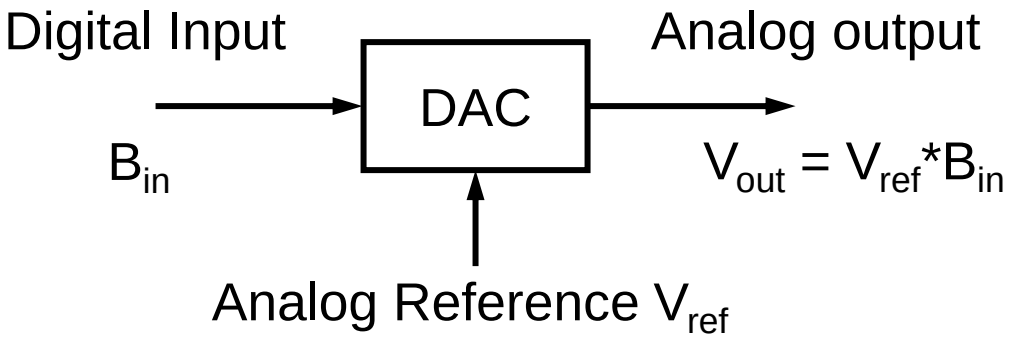
Ideal D/A Converter

- Ideal N-bit DAC
  - Digital input $B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$

    where b_i is 1 or 0, i.e. binary

    b_1 is the most significant bit (MSB)

    b_N is the last significant bit (LSB)



- A unipolar DAC produces an output signal of only one polarity.
- A signed (or bipolar) DAC produce an output of either positive or negative polarity, depending on a sign bit, usually b_1.
- Other digital (or analog) representation may be used

  (e.g. sign magnitude, offset binary, or 2's complement, ...etc.)
- We assume here that DAC is unipolar (for simplicity).

Ideal D/A Converter (Cont.)

- Analog output, V_{out}, is related to B_{in} through an analog reference, V_{ref}.
  - V_{out} and V_{ref} may be voltage, current, or charge.
  - We assume here that they are voltage (for simplicity)
  - Definitions:

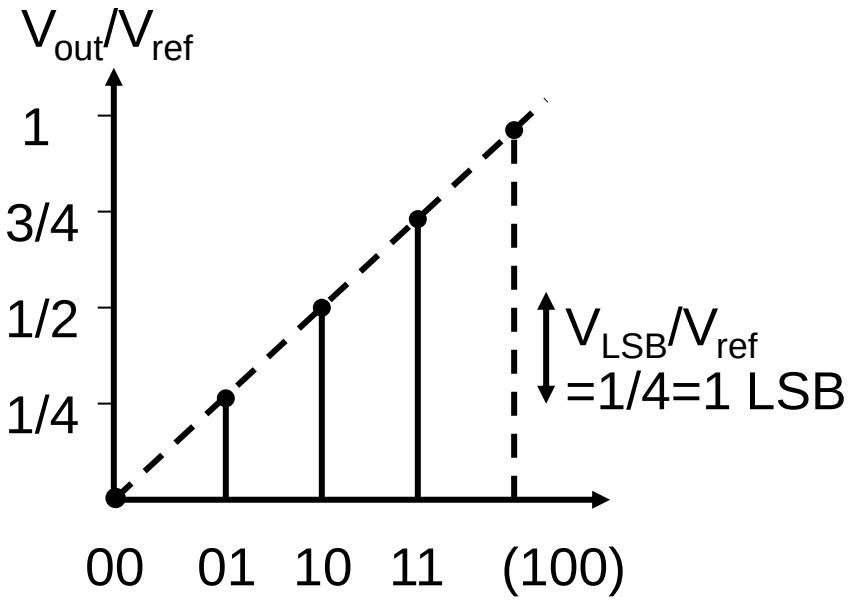
    $V_{out} = V_{ref} (b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{ref} * B_{in}$

    $V_{LSB} = V_{ref}/2^N$ where V_{LSB} is defined as the voltage changes when one LSB changes

    1LSB = $1/2^N$ unitless definition

Ideal D/A Converter (Cont.)

- An ideal 2-bit DAC example:
  Input-output transfer curve.
  In general, the maximum value of V_{out} is not V_{ref} but rather $V_{ref}(1 - 2^{-N})$, or equivalently, $V_{ref} - V_{LSB}$.



- A multiplying DAC (MDAC) is realized by simply allowing the reference signal, V_{ref} , to be a varying input signal along with B_{in}. Such an arrangement results in V_{out} being proportional to the multiplication of the input signals, B_{in} and V_{ref}.

Ideal A/D Converter

- Ideal N-bit ADC
  - Relations between external signals

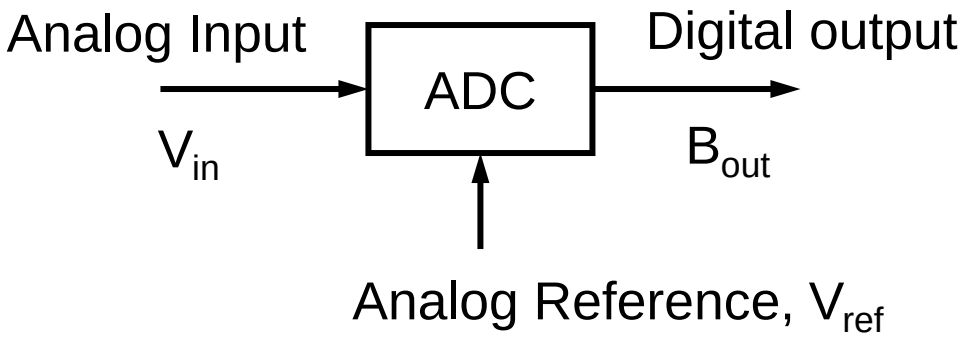
    $V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots\ldots + b_N 2^{-N}) = V_{in} \pm V_x$

    where $b_1 2^{-1} + b_2 2^{-2} + \ldots\ldots + b_N 2^{-N} = B_{out}$ is the digital output.

    V_{in} is analog input

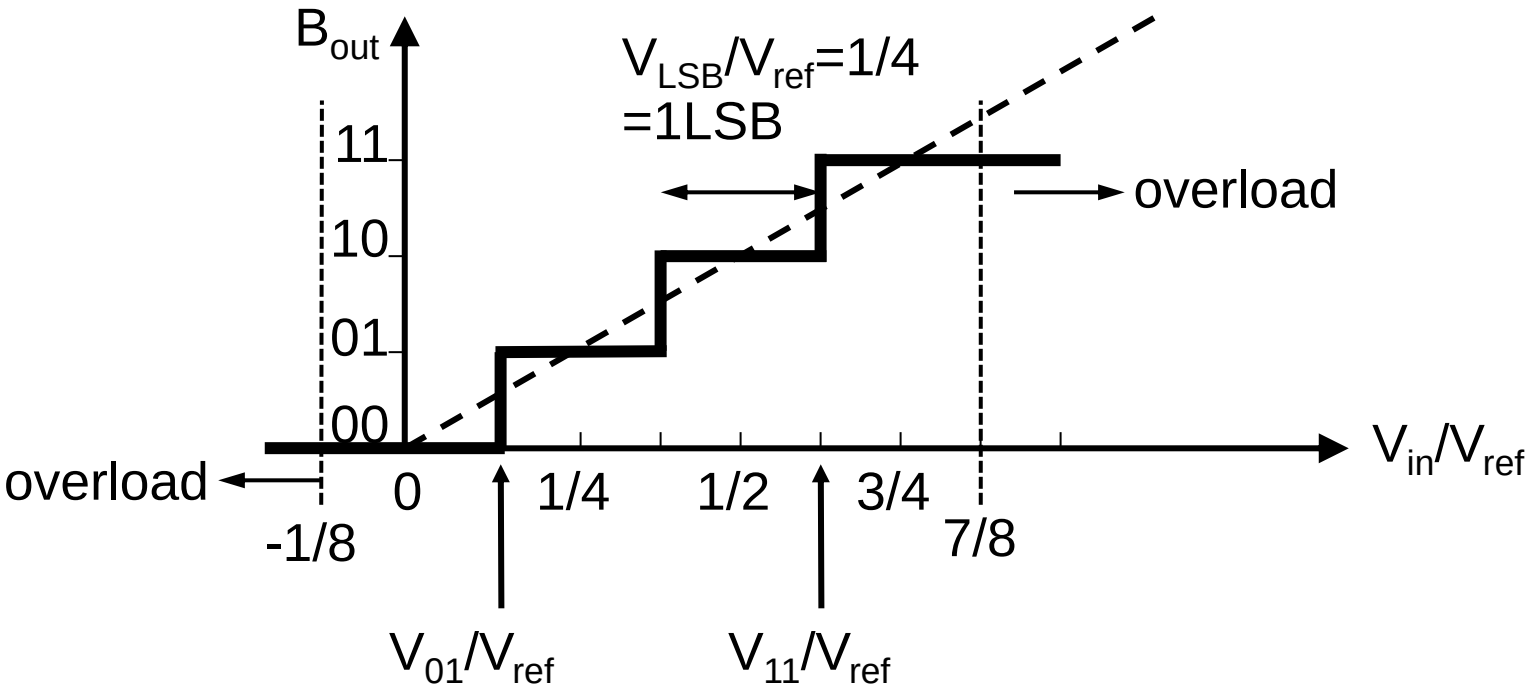
    V_{ref} is analog reference signal

    V_x is quantization error and $-1/2V_{LSB} \le V_x \le 1/2V_{LSB}$



Ideal A/D Converter (Cont.)

- Input-output transfer curve of an ideal 2-bit ADC
  - Transitions along the V_{in} axis are offset by $1/2V_{LSB}$ so that the midpoints of the staircase curve fall precisely on the equivalent D/A transfer curve.



Ideal A/D Converter (Cont.)

- Transition voltages at V_{ij} where the subscript ij indicates the upper B_{out} value of the transition, e.g. V_{01} is the transition from 00 to 01.

- $-1/8V_{ref} < V_{in} < 7/8V_{ref}$

  Otherwise, the quantizer is said to be overloaded since the magnitude of the quantization error would be larger than 1/2LSB.

Quantization Error in Ideal ADCs and DACs

- Ideal ADC
  - In the range of [-1/2LSB,1/2LSB].
- Ideal DAC
  - N-bit input for N-bit DAC

    No quantization error occurs
  - M-bit input for N-bit DAC(N>M)

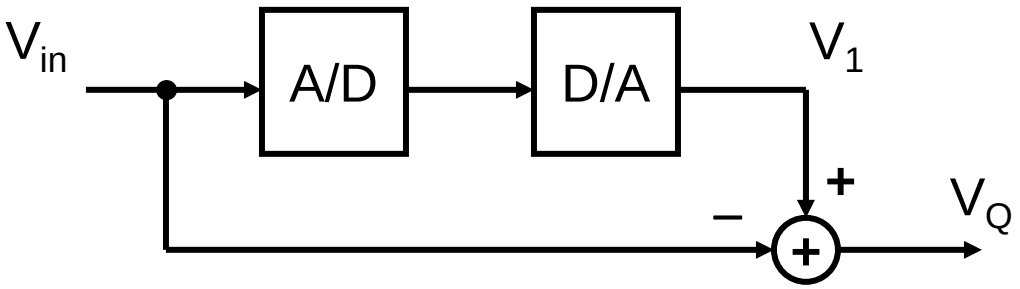
    No quantization error
  - M-bit input for N-bit DAC(N<M)

    In the range of [$-(1-1/2^{M-N})$LSB, $(1-1/2^{M-N})$LSB]

    Quantization errors occurs in the conversion from an M-bit digital signal to a N-bit digital signal.

Quantization Noise in Ideal ADCs

- Circuit to investigate quantization noise behavior



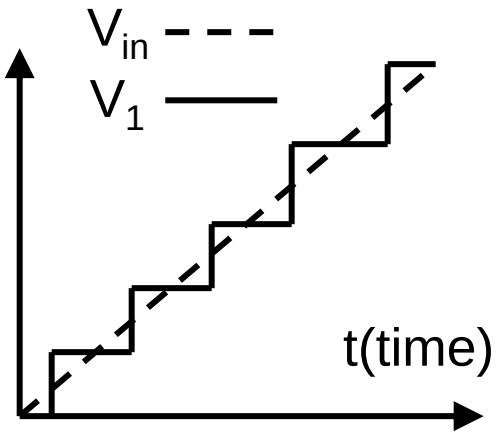
$$V_Q = V_1 - V_{in}$$

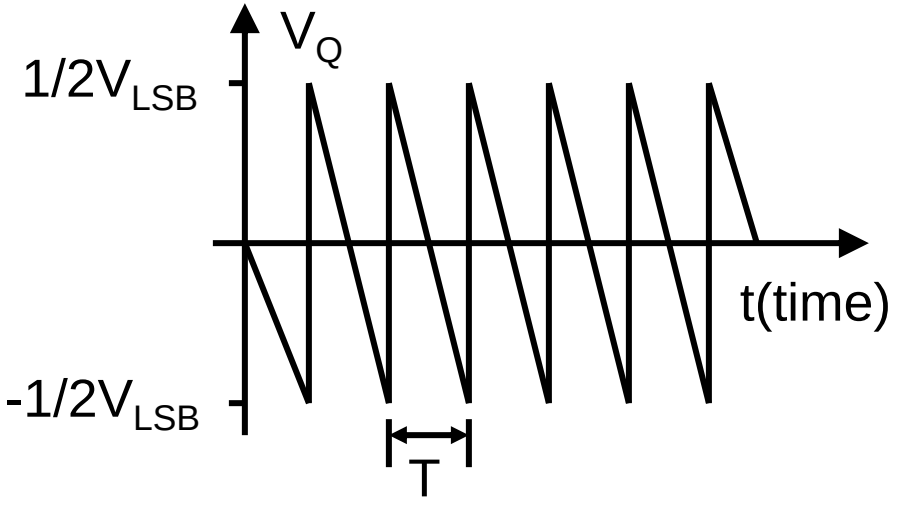
or $$V_1 = V_{in} + V_Q$$

  - Quantization noise can be modeled as the input signal, V_{in}, plus some additional quantization noise signal, V_Q .

Quantization Noise in Ideal ADCs (Cont.)

- Calculation of quantization noise
  - Deterministic approach
    - Assume the V_{in} is an ramp and such an input signal results in the output V_1 appearing as a staircase (no overloading is assumed). Taking the difference between V_{in} and V_1 gives us V_Q, which is quantization error V_Q is limited to ± 1/2LSB.





Quantization Noise in Ideal ADCs (Cont.)

- The average of V_Q is zero

  Root mean square (rms) value V_Q(rms)

$$V_{Q(rms)} = [\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2 dt]^{1/2} = [\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2 (-t/T)^2 dt]^{1/2}$$

$$= [\frac{V_{LSB}^2}{T^3}](\frac{t^3}{3})\Big|_{-T/2}^{T/2}]^{1/2} = V_{LSB}/\sqrt{12}$$

  ⇨ V_Q is proportional to the size of V_{LSB}, which is determined by bit number N.

- Stochastic approach

  To deal with more general input case, a stochastic approach is typically used.

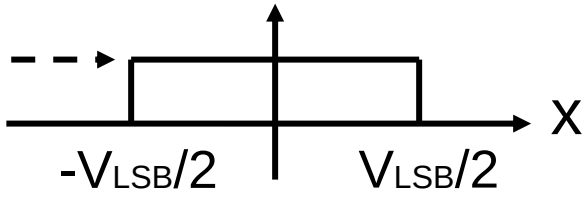
  - Assume that the input signal is varying rapidly such that V_Q is a random variable uniformly distributed between $\pm 1/2V_{LSB}$.

Quantization Noise in Ideal ADC (Cont.)

The probability density function $f_Q(x)$

$$f_Q(x) = 1/V_{LSB} \qquad \text{where } -1/2V_{LSB} < x < 1/2V_{LSB}$$

$$\int_{-\infty}^{\infty} f_Q(x)dx = 1$$



- The average value of V_Q is zero

$$V_{Q(avg)} = \int_{-\infty}^{\infty} xf_Q(x)dx = 1/V_{LSB}\int_{-V_{LSB/2}}^{V_{LSB/2}} xdx = 0$$

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_Q(x)dx\right]^{1/2}$$

$$= \left[1/V_{LSB}\left(\int_{-V_{LSB/2}}^{V_{LSB/2}} x^2dx\right)\right]^{1/2} = V_{LSB}/\sqrt{12}$$

which are the same as those found using the deterministic ramp input.

Quantization Noise in Ideal ADCs (Cont.)

- (i) Assume V_{in} is a sawtooth of height V_{ref} (or a random signal uniformly distributed between 0 and V_{ref} , the SNR

$$\mathrm{SNR} = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log(2^N) = 6.02\mathrm{NdB}$$

(ii) A more common SNR formula is to assume V_{in} is a sinusoidal waveform between 0 and V_{ref} .

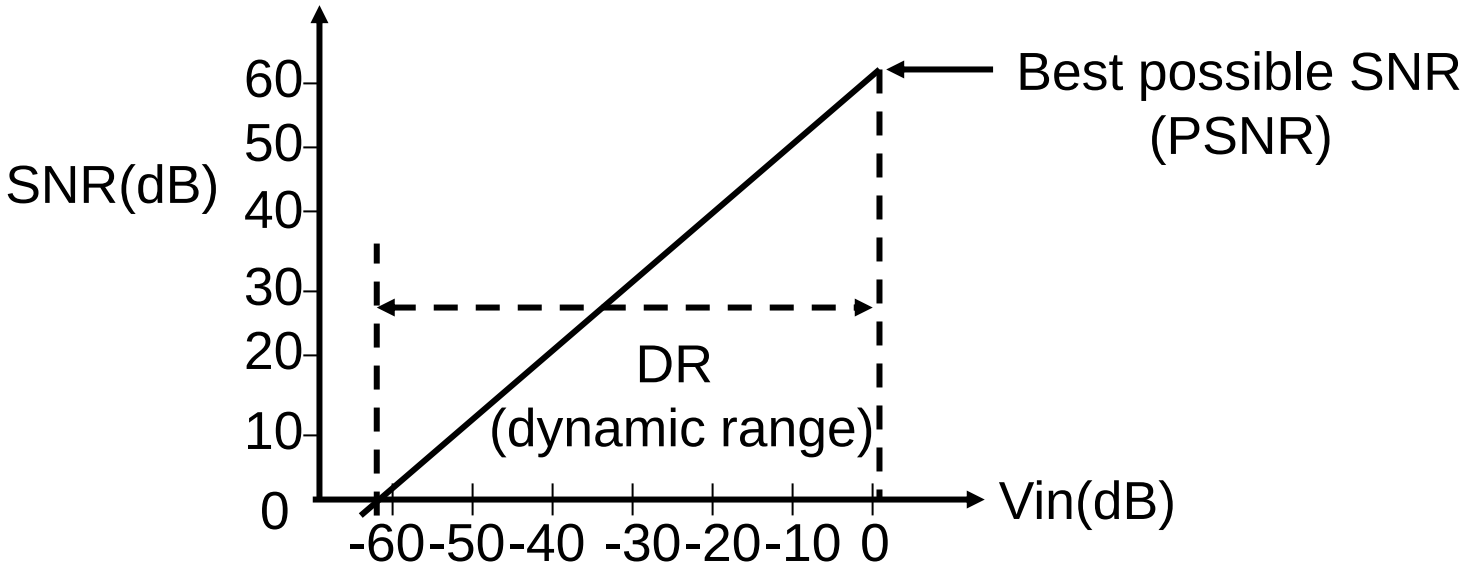
$$\mathrm{SNR} = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(\sqrt{\frac{3}{2}}2^N\right)$$

$$= 6.02\mathrm{N} + 1.76\mathrm{dB}$$

In other words, a sinusoidal signal has 1.76dB more ac power than a random signal uniformly distributed between the same peak levels. This equation gives the best possible SNR for an N-bit ADC. The maximum SNR can be achieved is also called peak signal-to-noise ratio (PSNR).

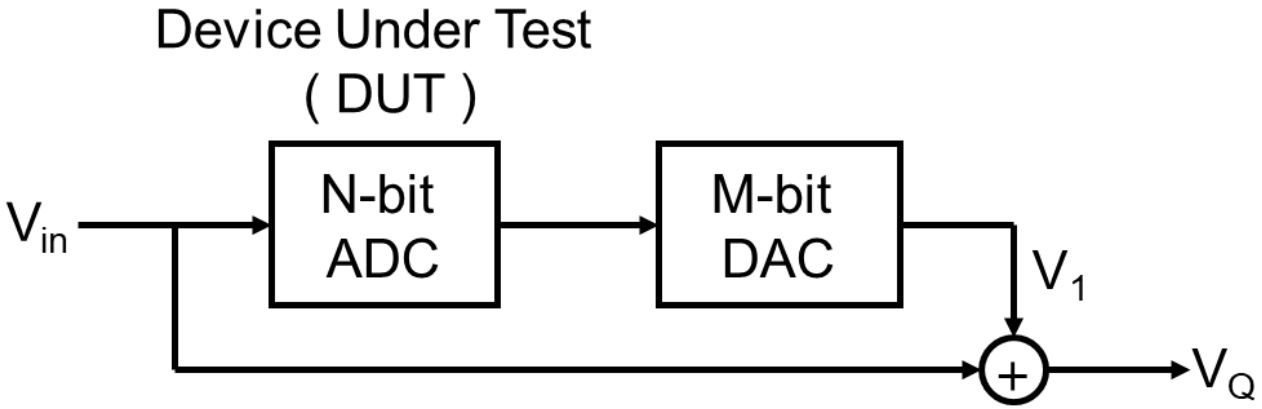
Quantization Noise in Ideal ADCs (Cont.)

- (iii) SNR vs. V_{in} plot (sine input and ideal 10-bit input for this example)



Practical Method for Measuring Errors in real ADCs

- ADC and DAC both are not ideal.
  ADC is the device under test.



  - Quantization error depending on how accurate the M-bit DAC is.
  - M-bit DAC has accuracy higher than N-bit.
  - V_Q can be further corrected
    - Subrange ADC (p.12-51)
    - Pipelined ADC (p.12-62)
    - Cyclic ADC (p.12-60)

Signed Codes

- Sign magnitude
- 1’s complement
- Offset binary
- 2’s complement
  - If many numbers are being added using 2’s complement codes, no overflow hardwire is required as long as the final result is within the digital range (even if the intermediate results go well out of range.)
  - A+B and A-B can be easily realized (refer to the textbook)

- Gray code
  - Often used for high speed communication systems.

Signed Codes (Cont.)

4 bits signed digital representations

Number	Normalized Number	Sign Magnitude	1's Complement	Offset Binary	2's Complement	Gray code
+7	+7/8	0111	0111	1111	0111	1000
+6	+6/8	0110	0110	1110	0110	1001
+5	+5/8	0101	0101	1101	0101	1011
+4	+4/8	0100	0100	1100	0100	1010
+3	+3/8	0011	0011	1011	0011	1110
+2	+2/8	0010	0010	1010	0010	1111
+1	+1/8	0001	0001	1001	0001	1101
+0	+0	0000	0000	1000	0000	1100
(-0)	(0)	(1000)	(1111)			
-1	-1/8	1001	1110	0111	1111	0100
-2	-2/8	1010	1101	0110	1110	0101
-3	-3/8	1011	1100	0101	1101	0111
-4	-4/8	1100	1011	0100	1100	0110
-5	-5/8	1101	1010	0011	1011	0010
-6	-6/8	1110	1001	0010	1010	0011
-7	-7/8	1111	1000	0001	1001	0001
-8	-8/8			0000	1000	0000

Performance Limitation

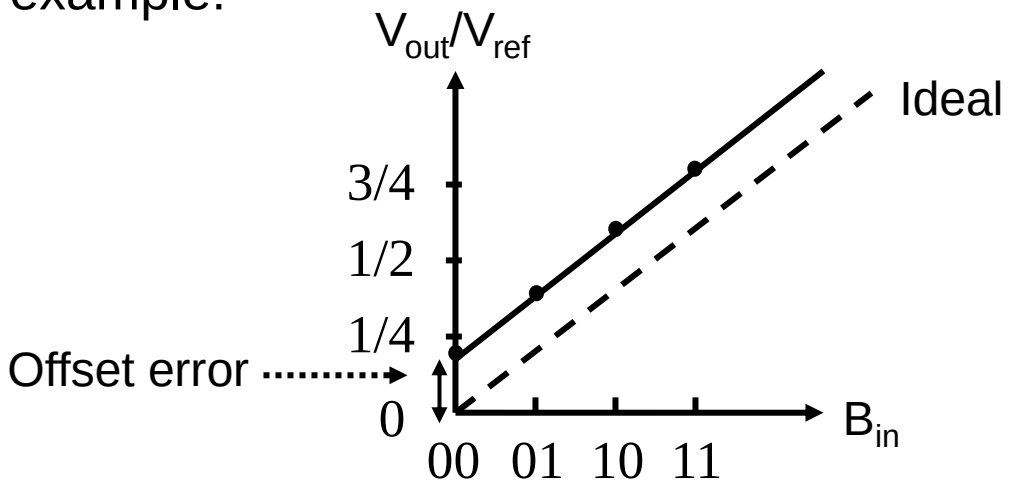
- Definitions for determining the transfer responses for both DACs & ADCs
  - DAC: The transfer response of a DAC is defined to be the analog levels that occur for each of the digital word.
  - ADC: The transfer response of an ADC can be defined as the analog transition point values, V_{ij} , we use the approach here.

- Resolution
  - The number of distinct analog levels corresponding to different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels.
  - Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.

Offset Error

- Offset error is in units of LSBs.
- DAC
  - Offset error is the output that occurs for the input code that should produce zero output .

    $E_{off(DAC)} = V_{out}/V_{LSB}\Big|_{0\ldots0}$
  - 2-bit example:

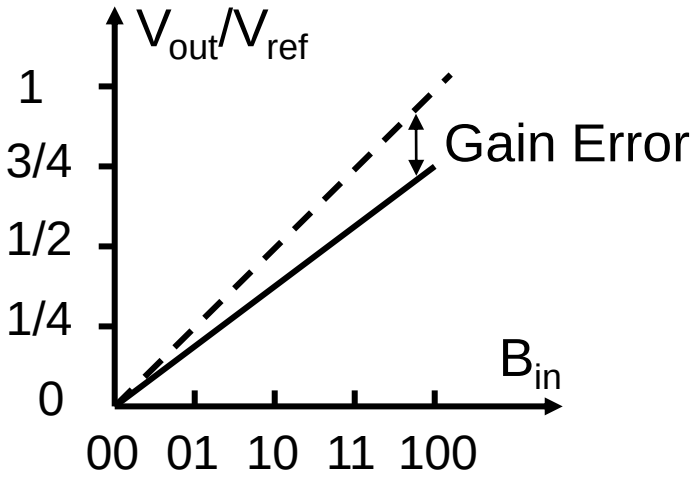


- ADC
  - Offset error is the deviation of $V_{0\ldots01}$ from 1/2LSB

    $E_{off(ADC)} = V_{0\ldots01}/V_{LSB}$ - 1/2LSB

Gain Error

- Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero.
- Gain error is in units of LSBs.
- DACs
  - $E_{gain(DAC)} = \left(\frac{V_{out}}{V_{LSB}}\Big|_{1\ldots1} - \frac{V_{out}}{V_{LSB}}\Big|_{0\ldots0}\right) - (2^N - 1)$
  - 2-bit example



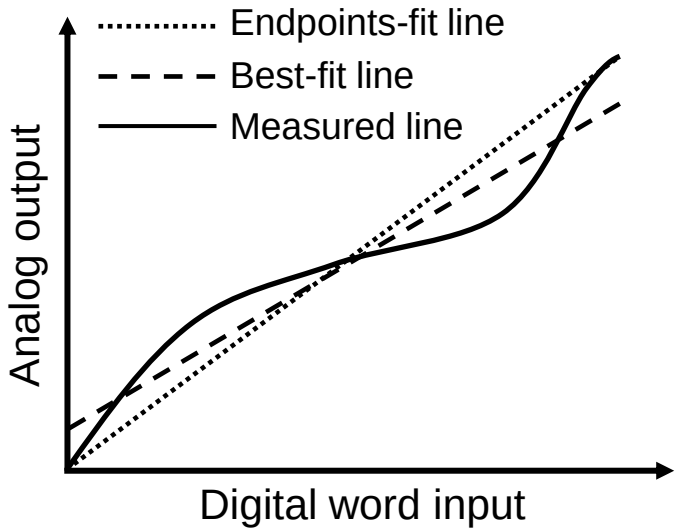
- ADC
  - $E_{gain(ADC)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots01}}{V_{LSB}}\right) - (2^N - 2)$

Accuracy

- Absolute accuracy
  - The difference between the expected and actual transfer responses.
  - 1. offset error, 2. gain error, and 3. linearity error (DNL、INL)
- Relative accuracy
  - The accuracy of offset and gain errors have been removed
- Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bit, or as a fraction of an LSB.
  - For example, a 12-bit accuracy implies that the converter's error is less than the full-scale divided by 2^{12} .
  - A converter may have 12-bit resolution with only 10-bit accuracy, or 10-bit resolution with 12-bit accuracy.
  - An accuracy greater than the resolution means that the converter's transfer response is very precisely controlled. (better than the number of bits of resolution).

Accuracy (Cont.)

- Integral Nonlinearity (INL) Error:
  - After both the offset and gain error have been removed, the integral nonlinearity (INL) error is defined to be the deviation from a straight line. However, what straight line should be used?



  - A conservative measure of nonlinearity is to use the endpoints of the converter's transfer response to define the straight. An alternate definition is to find the best-fit straight line such that the maximum difference (or perhaps the mean squared error) is minimized.
  - In general, the INL values are defined for each digital word. Sometimes, "INL" is defined as the maximum magnitude of INL values.

Accuracy (Cont.)

- Differential Nonlinearity (DNL) Error:
  - In an ideal converter, each analog step size is equal to LSB. In other words, in a D/A converter, each output level is 1 LSB from adjacent levels, whereas in A/D, the transition values are precisely 1 LSB apart.
  - Differential nonlinearity (DNL) is defined as the variation in analog step sizes away from 1LSB (typically, offset error have been removed).
  - Thus, an ideal converter has its maximum differential nonlinearity of 0 for all digital values, whereas a converter with a maximum differential nonlinearity of 0.5 LSB has its step size varying from 0.5LSB to 1.5LSB.
  - In general, as in the INL case, DNL values are defined for each digital word, whereas sometimes DNL is defined as the maximum magnitude of the DNL values.

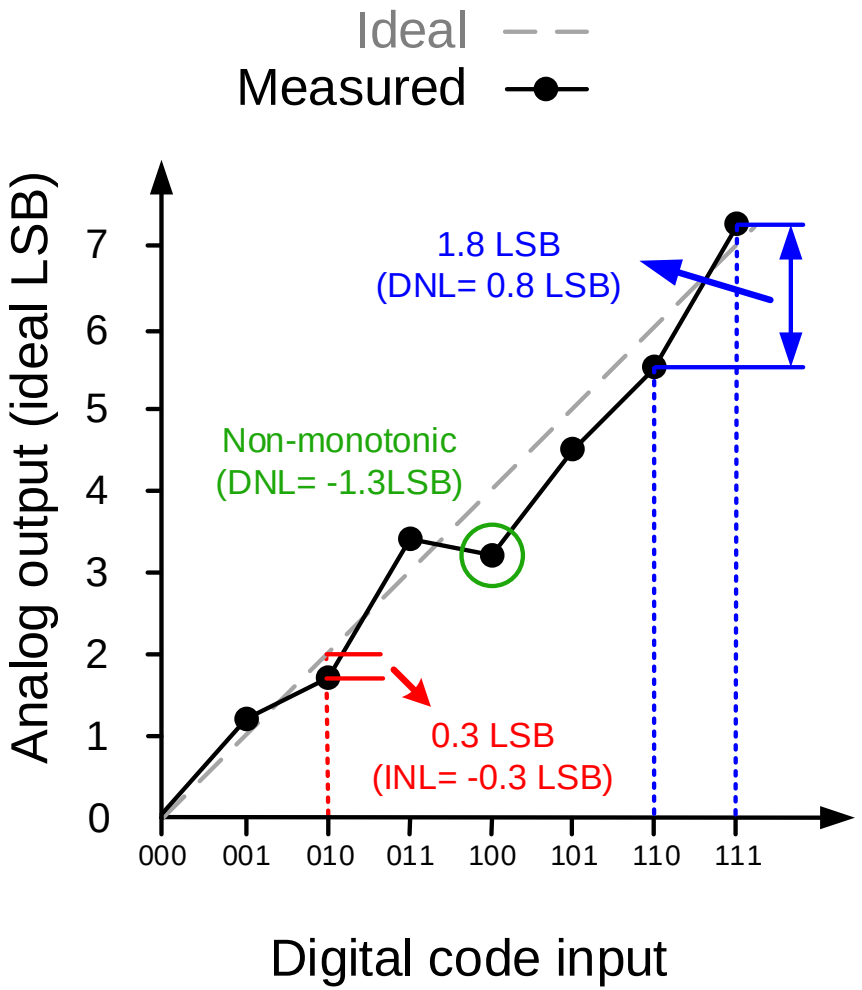
Accuracy (Cont.)

- Monotonicity:
  - A monotonic D/A is one in which the output always increase as the input increases. In other words, the slope of the D/A converter's transfer response is of only one sign.
  - If the maximum DNL error is less than 1LSB, then a D/A converter is guaranteed to be monotonic. However, many nonmonotonic converter may have a maximum DNL greater than 1 LSB. Similarly, a converter is guaranteed to be monotonic if the maximum INL is less than 0.5LSB.

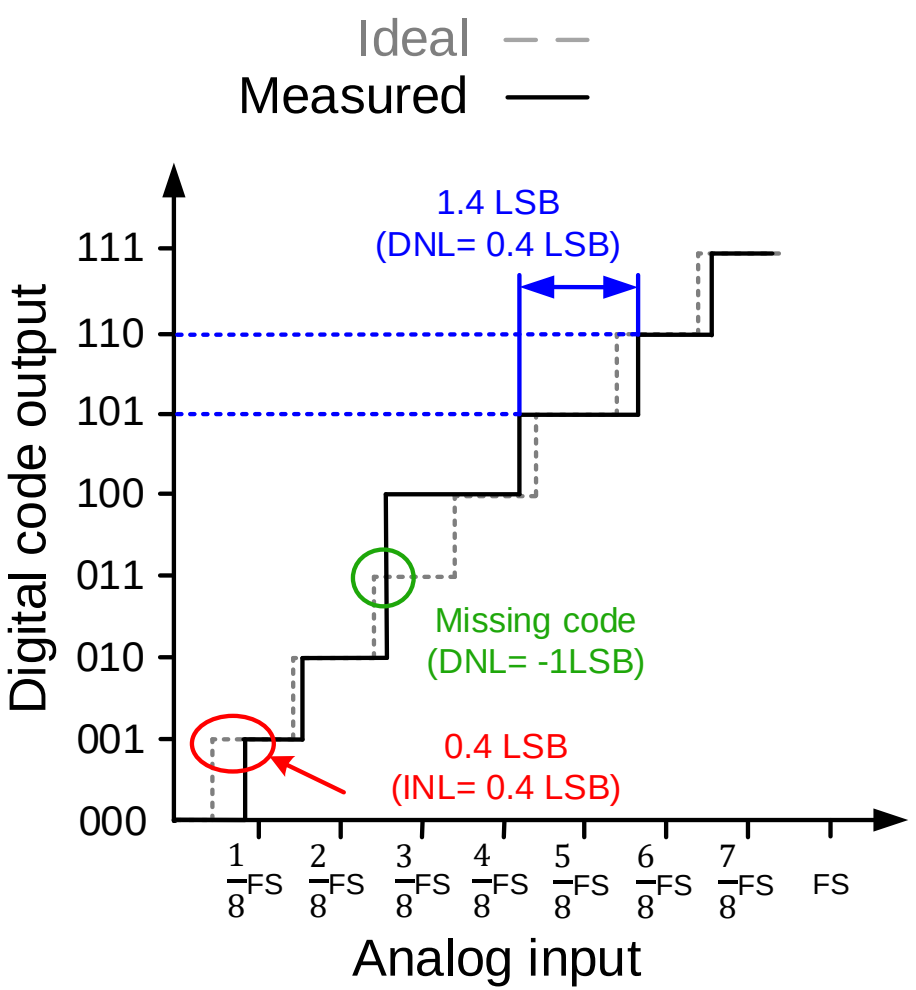
- Missing Codes:
  - Monotonicity is usually for D/A converters. An A/D converter is guaranteed not to have any missing codes if the maximum DNL error is less than 1LSB, i.e. monotonic.

Accuracy (Cont.)

- DAC transfer curve



- ADC transfer curve



Accuracy (Cont.)

- A/D Conversion Time and Sampling Rate:
  - Conversion time: The time for the converter to complete a single measurement including acquisition time for the input signal.
  - Sampling rate: The speed at which sampling can be continuously converted
    - Typically the inverse of the conversion time.
  - Some converters have a large latency between the input and the output due to pipelining or multiplexing, yet they still maintain a high sampling rate.
    - Example: A 12-bit 500kS/s pipeline ADC may have a conversion time of 2us yet a latency from input to output of 24us.

- D/A Settling Time and Sampling Rate :
  - Settling time: The time for the converter to settle within some specified amount of final value (usually 0.5LSB).
  - Sampling rate: The rate at which samples can be continuously converted
    - Typically the inverse of the settling time.

Accuracy (Cont.)

- Sampling Time Uncertainty (also known as aperture jitter):
  - Sampling instances are ill defined → ADCs & DACs have limited accuracy
  - Consider a full-scale signal V_{in} applied to an N-bits, signed, ADC with f_{in}

$$V_{in} = \frac{V_{ref}}{2}\sin(2\pi f_{in} t)$$

  - The slope of V_{in} at the peak of a sinusoidal waveform is small
    → Sampling time uncertainty is less of a problem near the peak values.
  - The maximum slope occurs at the zero crossing

$$\frac{dV_{in}}{dt}\Big|_{max} = \pi f_{in} V_{ref}$$

To keep ΔV due to some sampling-time uncertainty (Δt) less than $1V_{LSB}$

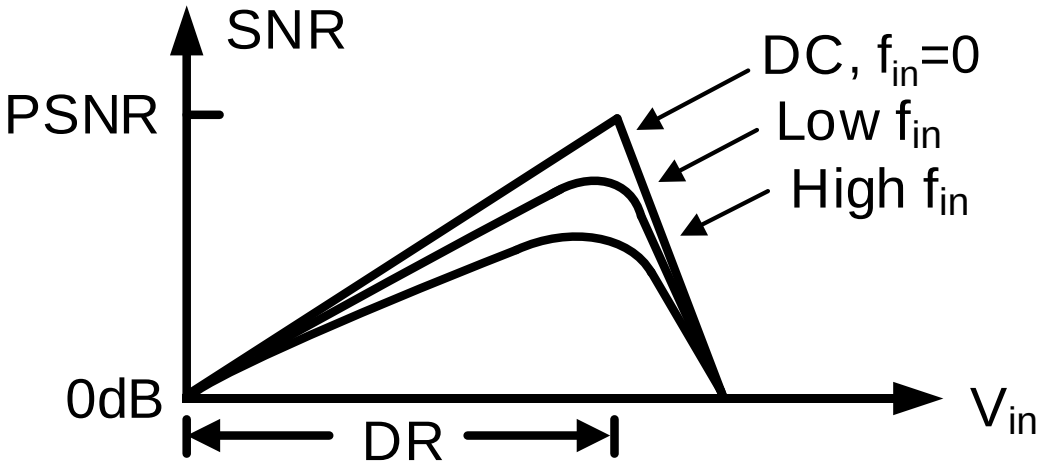
$$\frac{dV_{in}}{dt}\Big|_{max} < \frac{V_{LSB}}{\Delta t} \rightarrow \Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

Example: An 8-bit converter sampling a full-scale 250-MHz sinusoidal signal must keep its sampling-time uncertainty under 5ps to maintain 8-bit accuracy. Also, the same 5ps time accuracy is required for a 16-bit converter operating on a full-scale, 1-MHz signal.

Dynamic Range (DR)

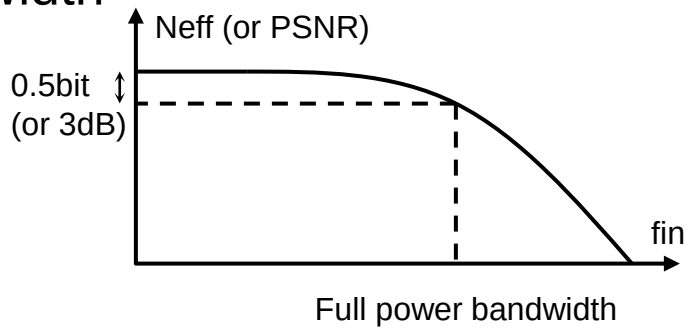
- Two different definitions:
  - The ratio of maximum amplitude input sinusoidal to minimum amplitude input sinusoidal.
    - Maximum input: input with PSNR or maximum allowable input.
    - Minimum input: input with SNR=0
  - Effective number of bit (N_{eff}), using the equation

    $PSNR = 6.02N_{eff} + 1.76dB$



Dynamic Range (Cont.)

- DAC
  - Analog output measured using spectrum analyzer
- ADC
  - Digital output analyzed using Fast Fourier Transform (FFT).
- Full-Power Bandwidth



- SNR is a function of the frequency of the sinusoidal input.
- For example, if an 8-bit, 200MHz A/D converter has a band-limited preamplifier or a slew rate limited sample and hold, dc input may show full 8-bit performance even at the maximum sample rate of 200M sample/s. However, a high-frequency sinusoidal input at, say, 40MHz, will require the input stage to track a rapidly varying signal and may result in only 6-bit performance.

Dynamic Range (Cont.)

- Distortion level (or Nonlinearity performance) of many converters
  - Remains at a fixed level and is not a function of input signal level
    - Input signal level ↓ ➔ signal-to-distortion ratio ↓
    - This behavior occurs because the distortion level is often determined by component matching and thus is fixed once the converter is realized.
  - Example: Most 1-bit oversampling converters have this desirable property since they do not rely on component matching and their distortion level is often a result of weak nonlinear effect at input stage.